Amendments to the Specification:

Amend page 2, paragraph beginning at line 13, as follows:

The present invention describes the architecture and implementation of a behavioral VHDL model of an ATM/SONET framer. The model is comprised of two independently configurable components, a Receiver and a Transmitter, and offers flexibility to allow testing with ~~multiple vendors' of~~ framers from multiple vendors by changing programmable parameters of the model.

Amend page 6, paragraph beginning at line 15, as follows:

The present invention describes the architecture and implementation of a behavioral VHDL model of an ATM/SONET framer. The model is comprised of two independently configurable components, a Receiver and a Transmitter, and offers flexibility to allow testing with ~~multiple vendors' of~~ framers from multiple vendors by changing programmable parameters of the model.

Amend page 10, paragraph beginning at line 18, as follows:

Many vendors' framers provide programmability in FIFO status update during Write and Read. A cell is generally not transmitted until the complete cell has been written into the Tx FIFO. The programmability feature allows the cell count to be incremented before the entire cell is physically transferred. This is specified in terms of number of words transferred across the UTOPIA interface. The model supports this programmability via a generic. Similarly, the cell count is decremented when a complete cell from Tx FIFO is inserted into the SONET frame. The cell count can be decremented at a programmable byte count into the ATM cell structure. This feature is also supported via a different generic. Two additional generics have been included in the model to mimic the synchronization delay between ATM and SONET clock domains. These two generics represent the latency associated with propagation and registration of FIFO status (cell count) update across the ATM/SONET domain boundary in each direction.